What is claimed is;

1. An IC chip comprising:

an electrode pad to which a re-wiring layer is not connected; and

a conductor post formed on the electrode pad.

2. The IC chip according to claim 1, wherein the conductor post is formed perpendicularly on the electrode pad.

3. The IC chip according to claim 1, wherein the conductor post has a crank shape or a zigzag shape.

4. The IC chip according to claim 1, wherein an inner portion of the conductor post is formed of a synthetic body, and a conductor material film is formed on an external surface of the conductor post.

5. The IC chip according to claim 1, wherein the conductor post comprises a first conductor post part, and a second conductor post part formed on the first conductor post part and made of solder.

6. The IC chip according to claim 5, wherein the first conductor post part and the second conductor post part have the same shape in cross section.

7. The IC chip according to claim 5, wherein the first conductor post part has a projection on the upper portion thereof.

8. The IC chip according to claim 7, wherein the projection has a shape where a capillary phenomenon occurs when dipped in a molten solder solution.

9. A connection construction of an IC chip comprising:

a first IC chip having a first electrode pad to which a re-wiring layer is not connected;

a second IC chip having a second electrode pad to which the re-wiring layer is connected;

wherein both the first electrode pad and the second electrode pad are connected to each other by a conductor post formed on the first electrode pad.

10. The connection construction of an IC chip according to claim 9, wherein the conductor post is formed perpendicularly on the first electrode pad.

11. The connection construction of an IC chip according to claim 9, wherein the conductor post has a crank shape or a zigzag shape.

12. The connection construction of an IC chip according to claim 9, wherein an inner portion of the conductor post is formed of a synthetic body, and a conductor material film is formed on an external surface of the conductor post.

13. The connection construction of an IC chip according to claim 9, wherein the conductor post comprises a first conductor post part, and a second conductor post part formed on the first conductor post part and made of solder.

14. The connection construction of an IC chip according to claim 9, wherein the first conductor post part and the second conductor post part have the same shape in cross section.

15. The connection construction of an IC chip according to claim 13, wherein the first conductor post part has a projection on the upper portion thereof.

16. The connection construction of an IC chip according to claim 15, wherein the projection has a shape where a capillary phenomenon occurs when dipped in a molten solder solution.

17. A method of fabricating an IC chip comprising the steps of:

laminating a first insulating layer on a board;

forming an electrode pad serving as an input/output terminal;

laminating a second insulating layer;

forming a resist pattern on the second insulating layer at a region excepting a part of the electrode pad;

etching and removing the second insulating layer while the resist pattern serves as a mask, thereby defining an opening in the second insulating layer on the electrode pad;

filling the opening with a conductive material layer made of a conductive material;

laminating a third insulating layer;

forming a resist pattern on the third insulating layer at a region excepting a region of the conductive material layer;

etching and removing the third insulating layer while the resist pattern serves as a mask, thereby defining an opening in the third insulating layer at the region of the conductive material layer;

filling the opening with a metal layer made of an electric connection material; and

etching and removing the third insulating layer and the second insulating layer.

18. The method of fabricating an IC chip according to claim 17, wherein the electric connection material is molten solder.

19. A method of fabricating an IC chip comprising the steps of:

laminating a first insulating layer on a board;

forming an electrode pad serving as an input/output terminal;

laminating a second insulating layer;

forming a resist pattern on the second insulating layer at a region excepting a part of the electrode pad;

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etching and removing the second insulating layer while the resist pattern serves as a mask, thereby defining an opening in the second insulating layer on the electrode pad;

filling the opening with a conductive material layer made of a conductive material; and

etching and removing the second insulating layer, thereby exposing the conductive material layer.

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20. The method of fabricating an IC chip according to claim 19, wherein a tip end of the exposed conductive material layer is dipped in a liquid bath filled with a molten electric connection material.

21. The method of fabricating an IC chip according to claim 19, wherein the electric connection material is molten solder.

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22. A method of probing a plurality of IC chips each formed on a wafer and having an electrode pad on which a conductor post is formed comprising effecting probing while a terminal of a probe is brought into contact with the conductor post formed on the electrode pad.

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23. The proving method according to claim 22, wherein the terminal of the probe has a planar shape.

24. The probing method according to claim 23, wherein a layout of the terminal of the probe is made by relatively conforming to a layout of the conductor post formed on the electrode pad of the IC chips.

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